REDUCING THE COMPLEXITIES AND INCREASING THE PRODUCTIVITY IN AUTOMOTIVE E/E ARCHITECTURE DESIGN

Use Case Studies with ModelCenter

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OUTLINE

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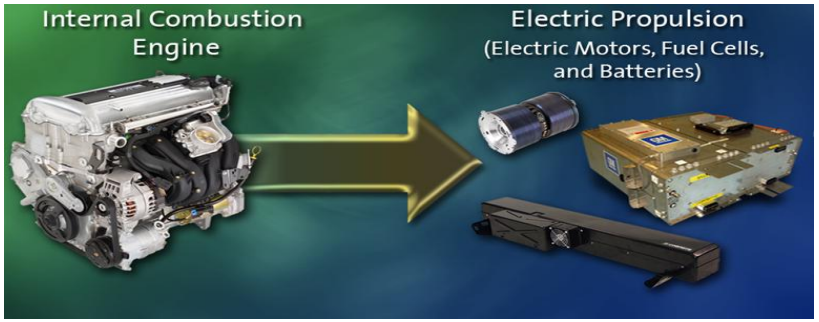
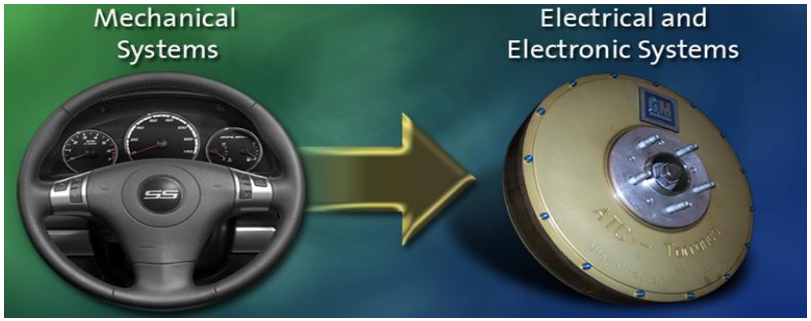
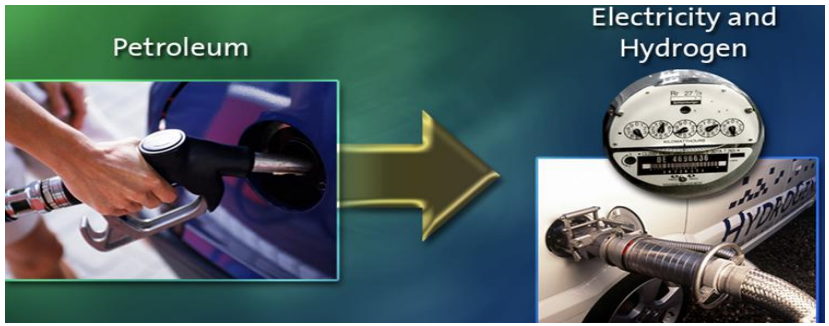
THE NEW VEHICLE DNA







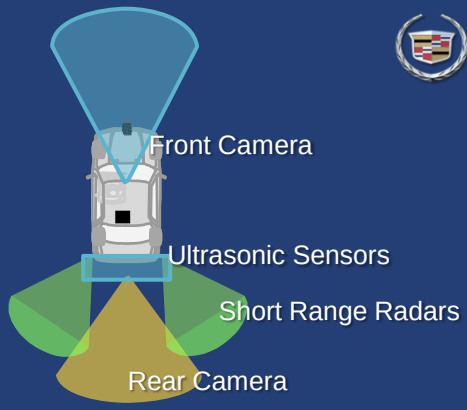
Totally Dependence on the Driver → **Semi/Full Autonomous Driving**

Vehicle Sized for Max Use – People and Cargo → **Vehicle Tailored to Specific Use**

CADILLAC DRIVER ASSISTANCE/ACTIVE SAFETY

Package 1: "Driver Awareness Package"

Cadillac ATS
Cadillac XTS
Cadillac SRX



Safety Alert Seat

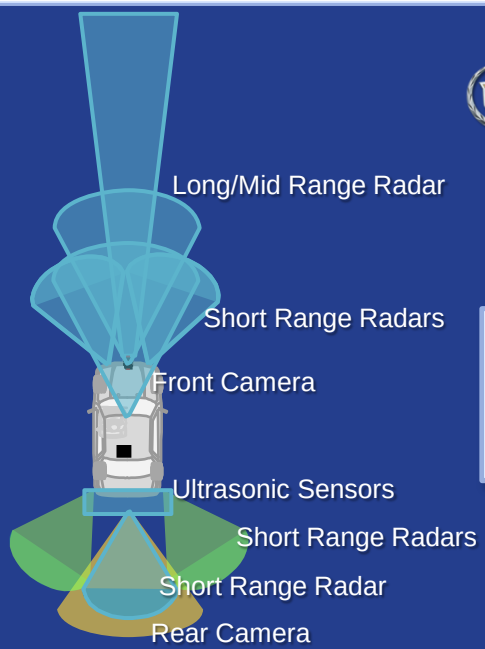
- Lane Departure Warning
- Forward Collision Alert
- Side Blind-Zone Alert
- Rear Cross-Traffic Alert
- Haptic Safety Alert Seat Feedback

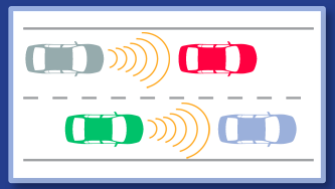
Also includes:

- Rear Vision Camera
- Front & Rear Park Assist

Package 2: "Driver Assist Package"

Cadillac ATS
Cadillac XTS
Cadillac SRX

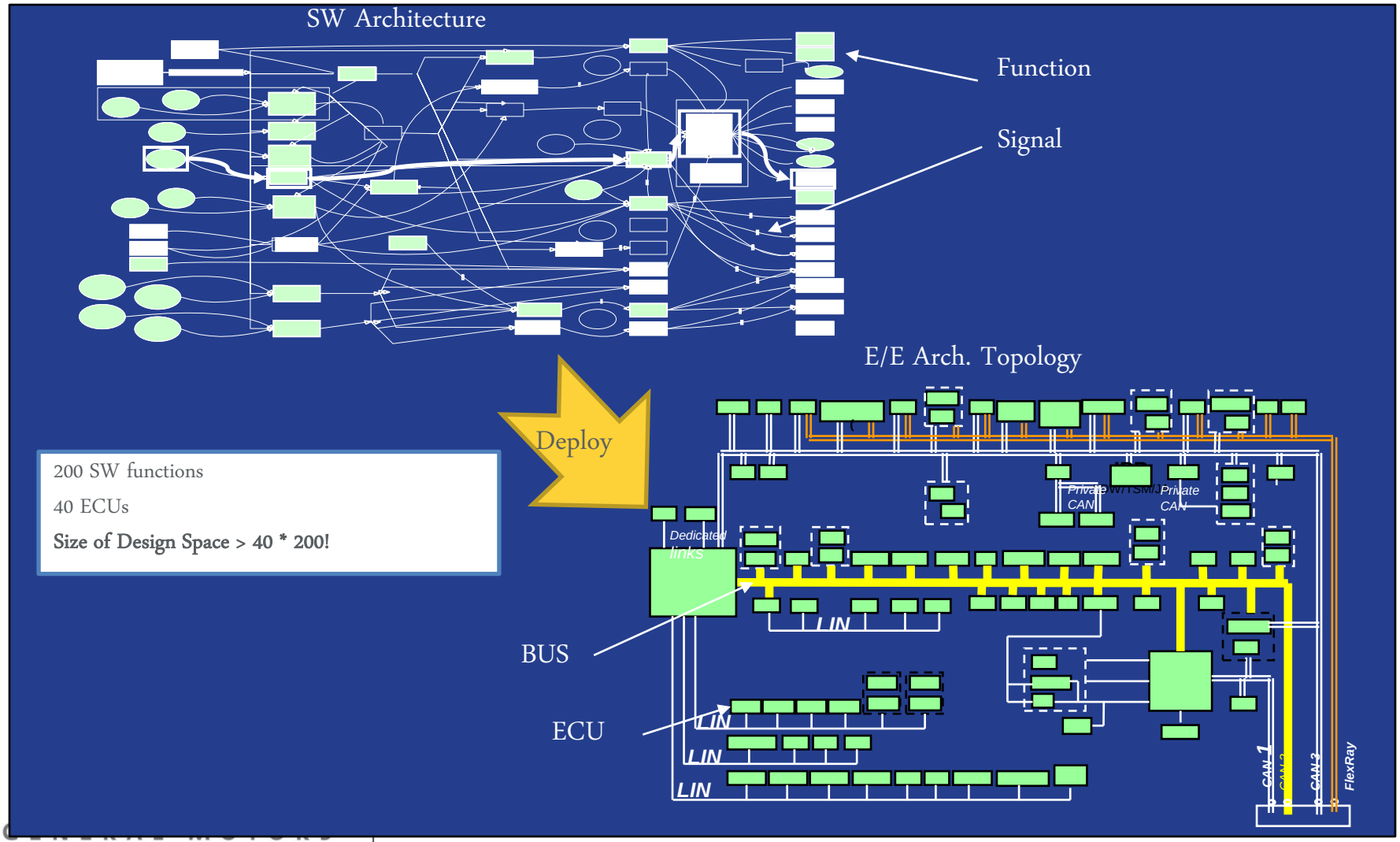




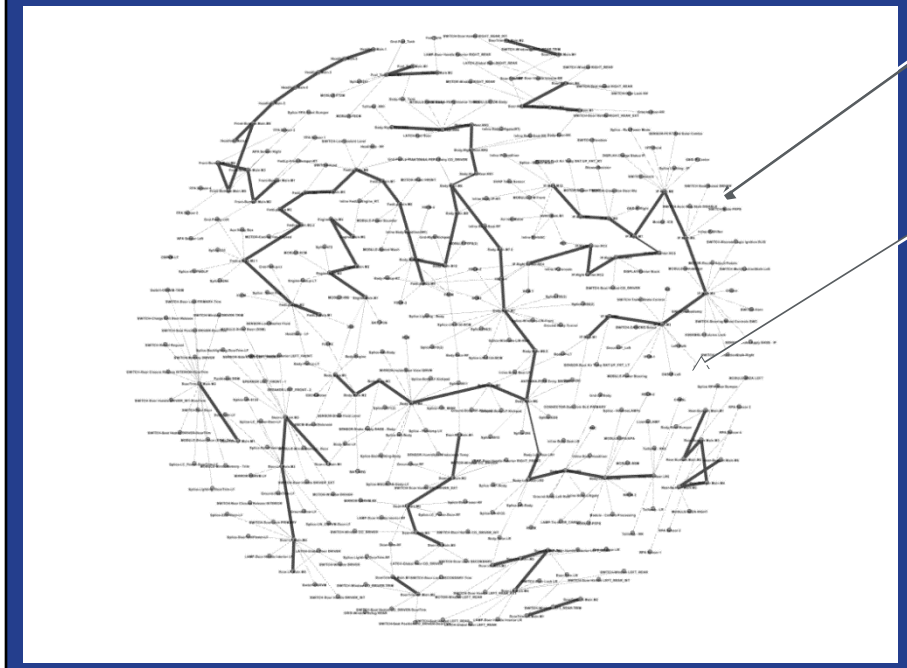
Package 1 plus:

- Full Speed-Range ACC (Stop w/Go Notifier)
- Auto Collision Preparation (includes Collision Imminent Braking)
- Low-Speed Front/Rear Automatic Braking (Emergency Braking to Avoid Contact)

IN-VEHICLE SW/HW ARCHITECTURES COMPLEXITIES – LOGICAL VIEW



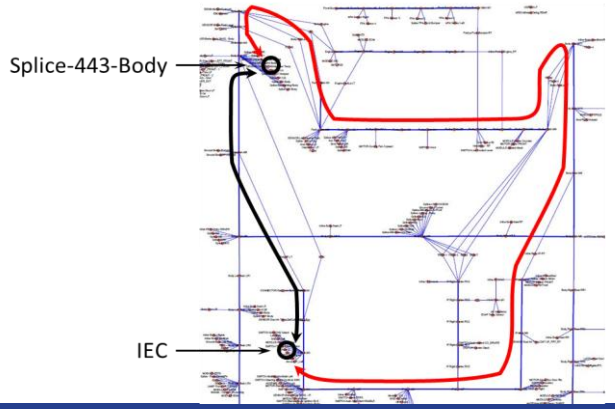
IN-VEHICLE SW/HW ARCHITECTURES COMPLEXITIES – WIRING HARNESS VIEW



Wiring Harness

Device
(ECU, Fuse Boxes, etc…)

Connection	Part 1	Part 2
1	IEC	Splice-443-Body



100 nets (device 2 device)

2 wiring routes/net

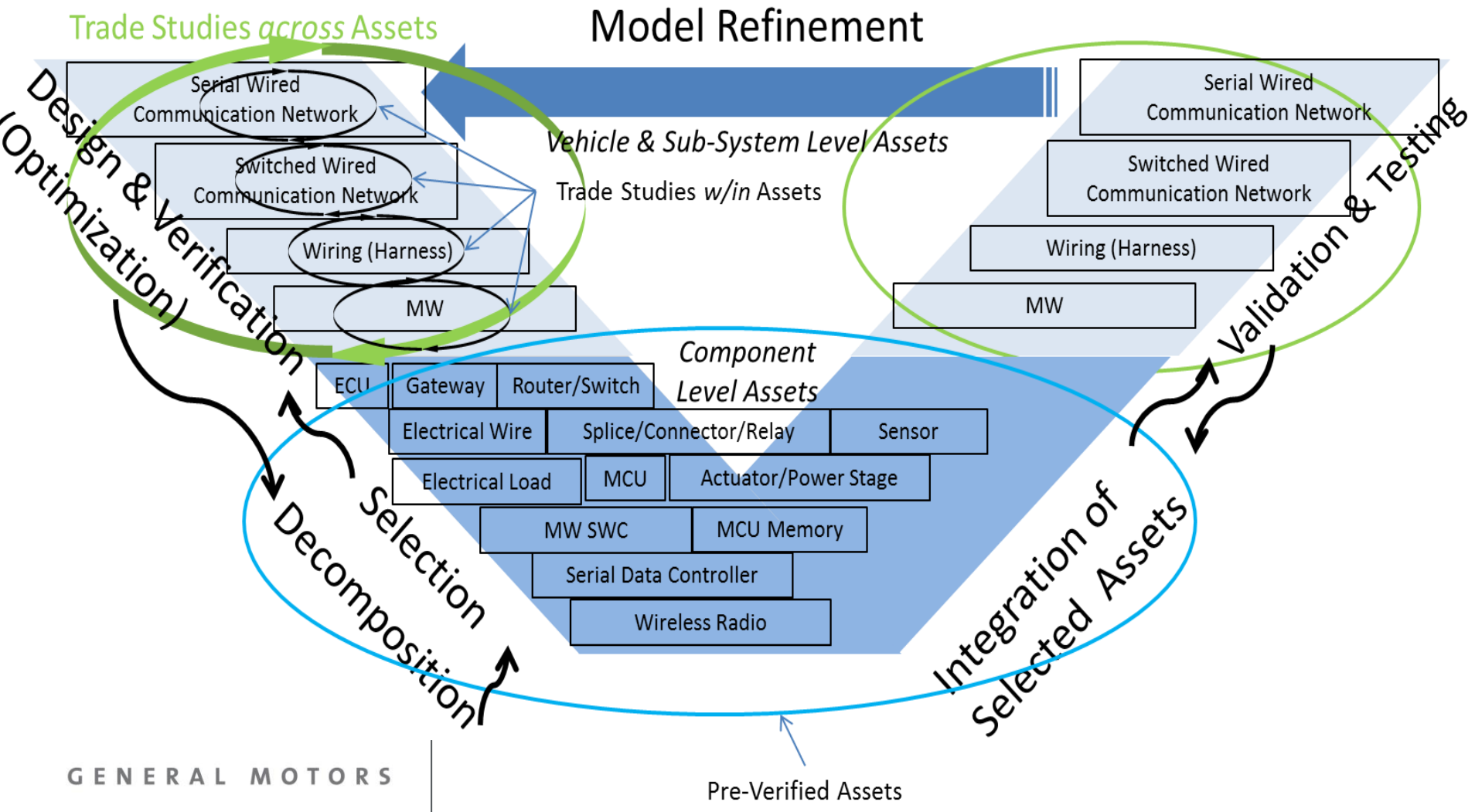
3 wire sizes/wire

Size of Design Space = 2^100 *3^100!

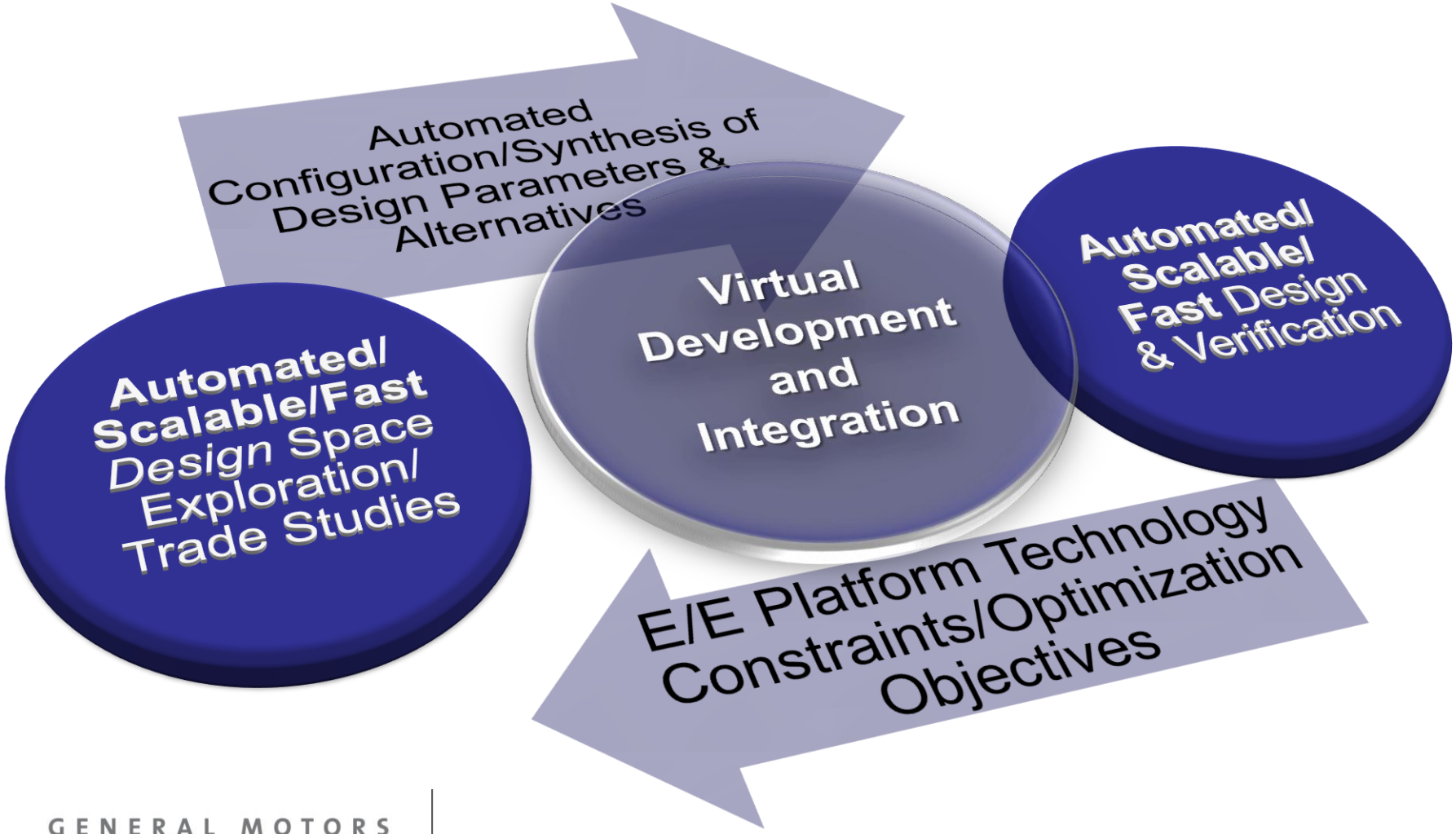
OUR OBJECTIVES

- Process Improvements
  - Manage/Reduce Design Complexities prior to the testing (simulation/bench/vehicle)
  - Reduce embedded control SW and E/E architecture development time and cost
  - Increase Design Space Exploration Throughput
- Product Improvements
  - Maximize Integrity, Safety, Security, and Performance
  - Increase MPG and Reduce CO2 Emissions
  - Reduce System and Part Costs/Mass
  - Strive for the Best Quality

OEM'S AUTOMOTIVE V-CYCLE – WHERE TO FRONT-LOAD THE TRADE-STUDIES

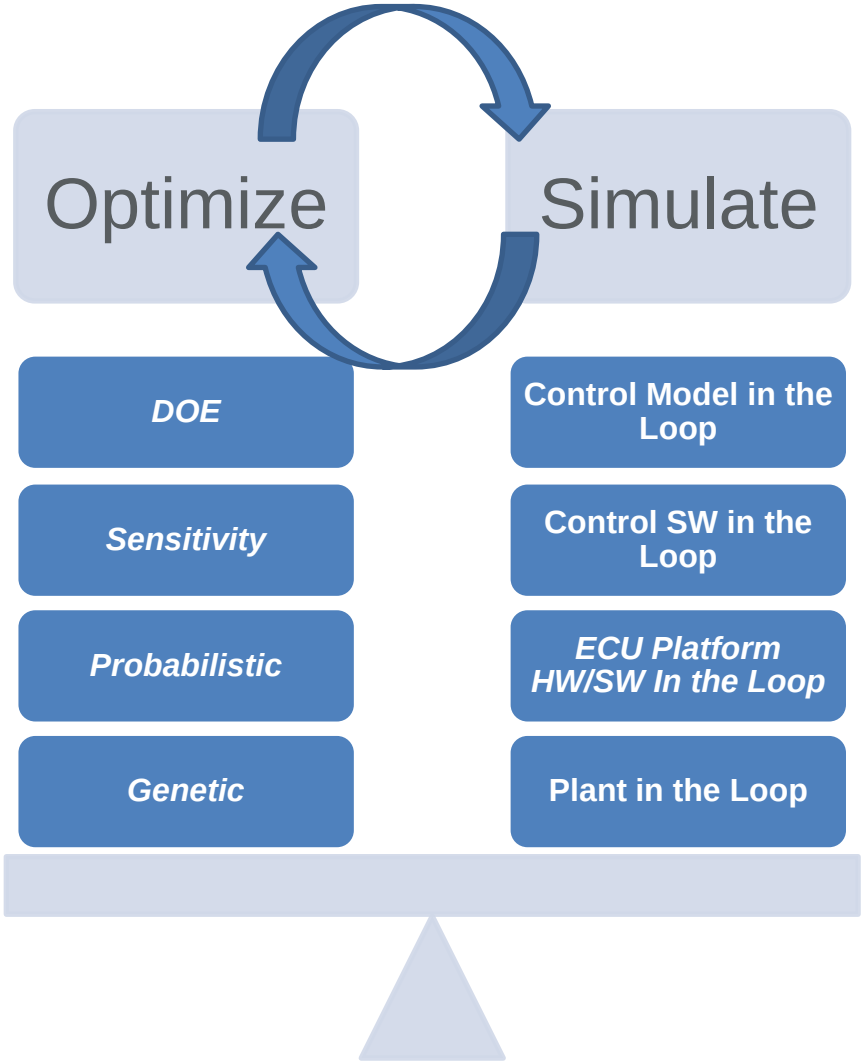


CAPABILITY STRATEGY

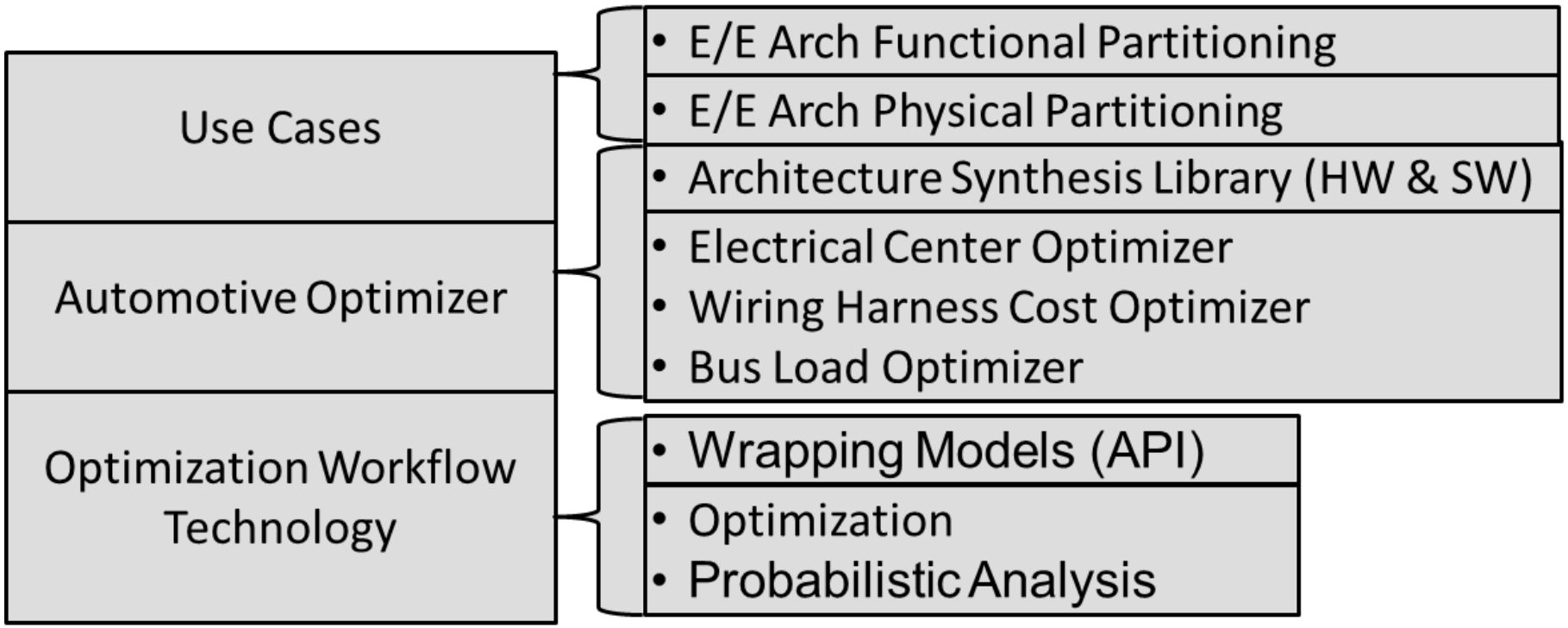


TOOL STRATEGY

- **Automated** exploration/optimization of ECS design alternatives
  - 👍 Reduction of design complexity, E/E Arch. BOM cost
- **Mixed-Fidelity** Integrated Modeling/Simulation of ECS assets with **ECU Platform HW/SW in the loop**
  - 👍 Early SW development & integration & testing



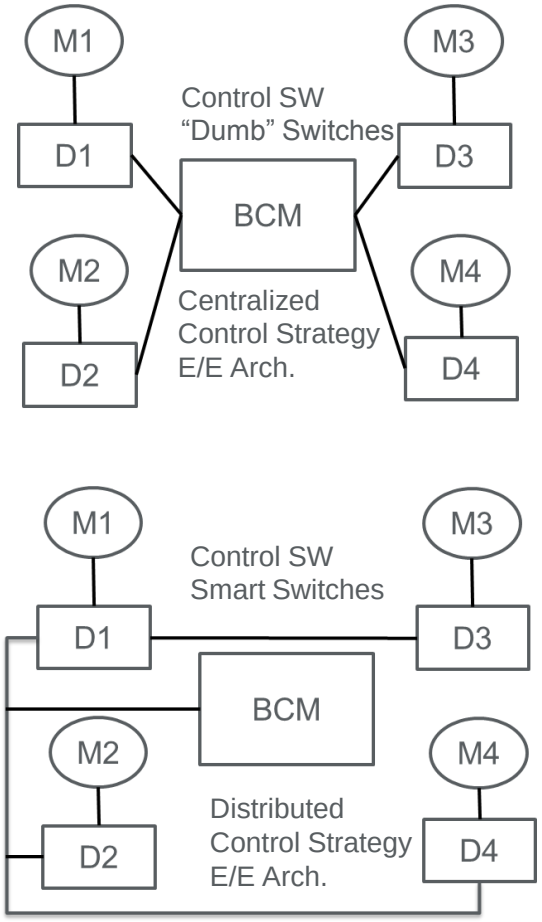
PLUG-AND-PLAY OPTIMZATION PLATFORM



CASE STUDY: POWER WINDOW DESIGN

Questions for the trade-study:

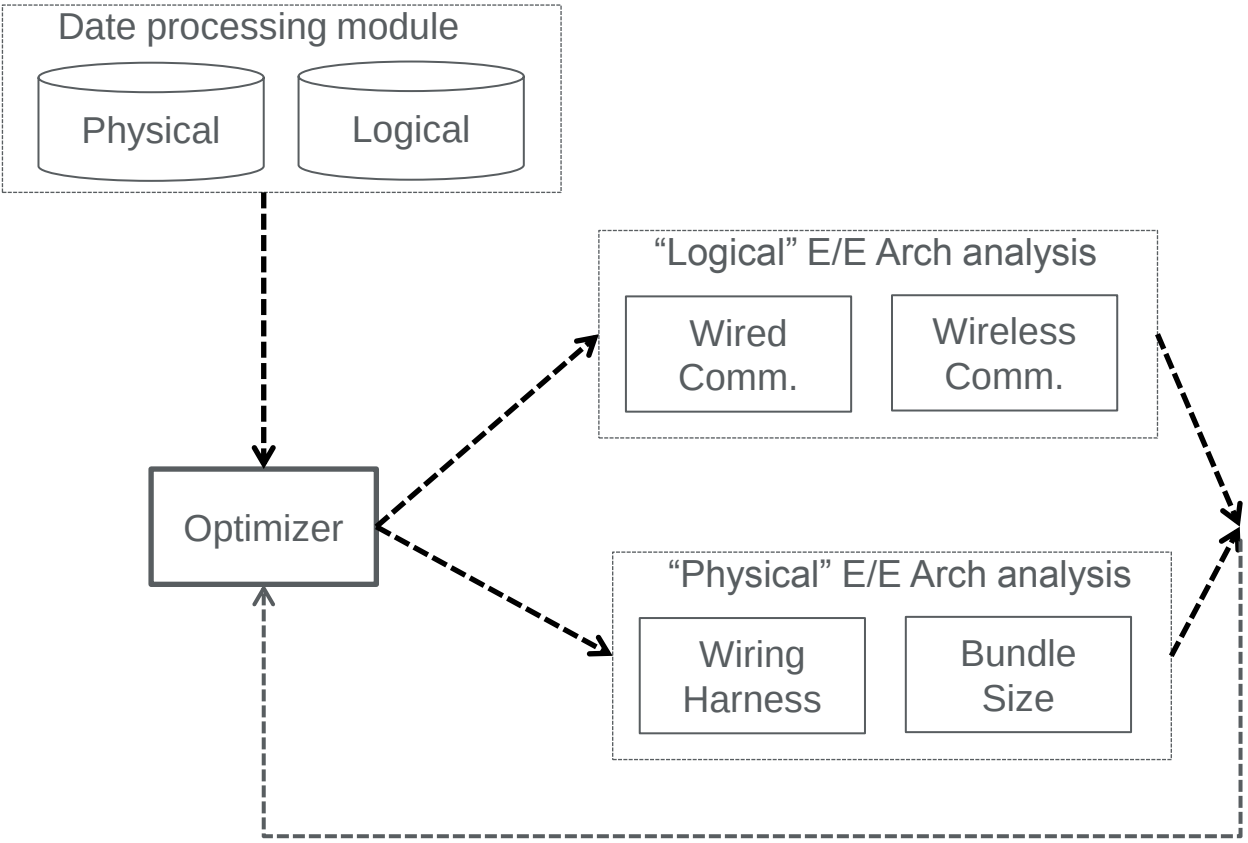
- Which design is more cost effective while feasible?
- Would a wireless communication link be a benefit?



Tool requirements:

- Architecture topology exploration
- Serial bus load analysis
- SW allocation

WORKFLOW FOR TRADE-STUDY

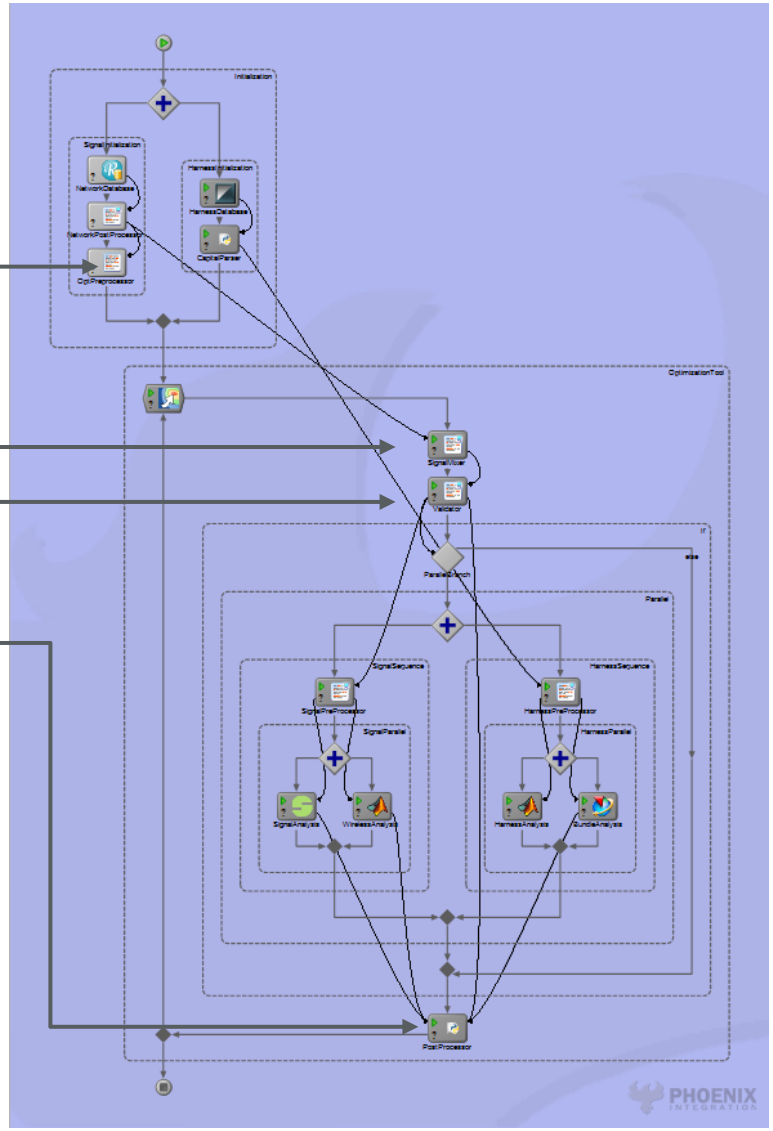


- **Objectives**
  - Min: cost, wired communication link load/latency
  - Max: wireless communication link reliability
- **Constraints**
  - Quality of service (response time, packet loss rate)
  - Wire resistance
  - Harness device allocation
  - E/E Architecture Topology
  - Wired communication link load
- **Design variables**
  - Architecture Topology & Software Allocation: topology includes ECUs/devices and ways of communicating (wireless or wired); selection of wireless radio technologies (Bluetooth or RFID)
  - Wire Size: depends upon load constraints
  - Wire Length: depends upon device allocation to harness

(SOME) WORKFLOW DETAILS

Optimization Related Scripts

- Optimization Preprocessor
  - Generates signal/ECU allocation alternative
  - Sets initial signal/ECU allocation
- Signal Mixer
  - Builds the network message
  - Passes wireless on/off
- Validator
  - Validates configuration
- Optimization Postprocessor
  - Merges wired/wireless results



Third Party Wrapped tools

- Mentor Graphics Capital
- IBM Rational Rhapsody
- SymTA/S
- MatLab
- NX

TAKEAWAYS

- Design is simple…The design space is huge!
- Explored ~3000 designs ($\sim 10^{59} \times 3^{8} \times 2 = 1.3 \times 10^{63}$ total design points) and determined the Pareto front
- Took 10 hours on a 4-core/4 GB machine
- Parallelization can dramatically increase the explored design space and computation efficiency

SIGNAL ANALYSIS

Signal Preprocessor

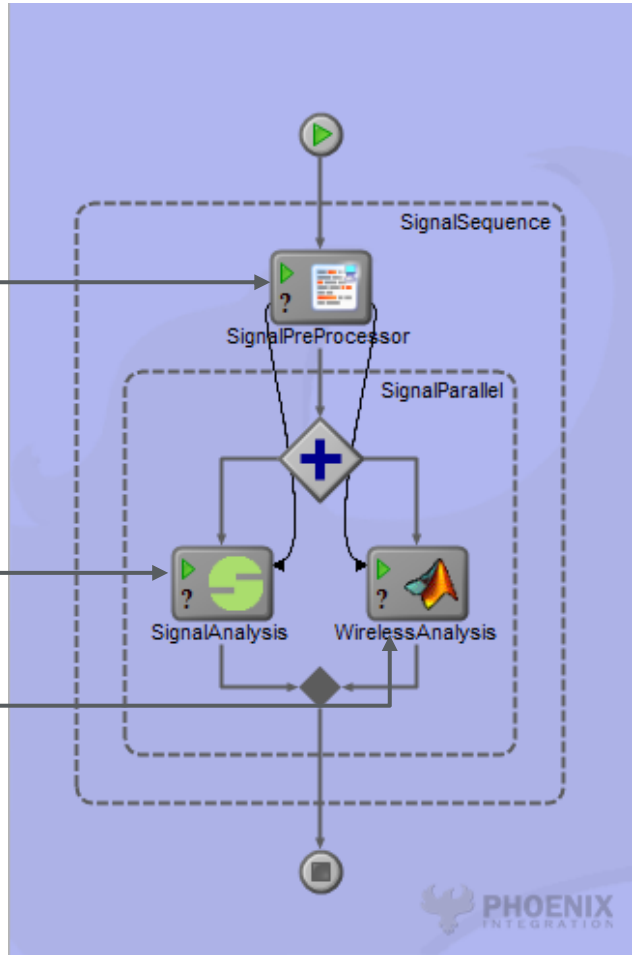
- Formats data from Rhapsody for SymTA/S

SymTA/S plug-in

- Builds and runs SymTA/S model
- Extracts event models from SymTA/S output

Wireless analysis

- Calculates response time and packet loss rate for wireless signals



CONCLUSIONS

- E/E Architectures are increasingly complex
- Need to reduce complexity to
  - Ease Testing
  - Reduce System and Part Cost
  - Increase Reliability
  - Strive for best Quality
- We have shown our capability and tool strategy
  - Optimization and Automated Worflows can play a major role in the strategy
- We have shown a use case study to support automated trade-study
- We strive to continue introducing system level trade-studies in our engineering development processes